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10/530,495	04/06/2005	Ramanathan Sethuraman	NL 020975	4791

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EXAMINER	
PETRANEK, JACOB ANDREW	
ART UNIT	**PAPER NUMBER**
2183	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/530,495	SETHURAMAN ET AL.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 14-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 14-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *4/6/2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-12 and 14-17 are pending.

2. The office acknowledges the following papers:

Claims and arguments filed on 7/9/2008.

Withdrawn objections and rejections

3. The claim objection for claim 14 is withdrawn due to amendment.

Claim objections

4. Claim 1 is objected to for the following reasons:

5. Claim 1 recites "the detection unit being coupled to the instruction execution unit parallelizes" that should be changed to "the detection unit being coupled to the instruction execution unit that parallelizes."

Drawing objections

6. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitations from claims 1-12 and 14-17 must be shown or the feature(s) canceled from the claim(s). The objection will be withdrawn when the figures are labeled with the claimed limitations. No new matter should be entered. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d).

New Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-5, 7, and 15-17 are rejected under 35 U.S.C. §103(a) as being unpatentable over Fisher et al. (U.S. 6,026, 479), in view of Jensen et al. (U.S. 7,149,878).

9. As per claim 1:

Fisher discloses a data processing apparatus the apparatus comprising:

an instruction memory address generation circuit for outputting an instruction address (Fisher: Figure 2 elements 120 and 122, column 5 lines 54-61)(The cache memory is inherently addressed by a program counter that generates an instruction address.);

an instruction memory system arranged to output an instruction word addressed by the instruction address (Fisher: Figure 2 elements 120 and 122, column 5 lines 54-61)(The caches are the instruction memory system. They inherently output instructions by instruction addresses generated by a program counter.), including at least one type of memory selected to achieve a desired instruction cycle time (Fisher: Figure 6 elements 620 and 622, column 8 lines 48-60)(The memory is selected to be a cache to achieve faster performance and access to the instructions.) wherein longer instruction

words are stored in said memory system within memory ranges of progressively shorter instruction words associated with

a corresponding memory type (Fisher: Figure 6 element 620 and 622, column 8 lines 41-65)(The high and low ILP instructions are stored within ranges stored in the instruction cache.);

an instruction execution unit, arranged to process a plurality of instruction from the instruction word in parallel (Fisher: Figure 2 elements 150A-D, column 5 lines 26-37)(The execution units process instructions in parallel for high ILP code.).

Fisher failed to teach a detection unit, arranged to detect in which of a plurality of ranges the instruction address lies, the detection unit being coupled to the instruction execution unit that parallelizes processing of the instructions from the instruction word, dependent on a detected range.

However, Jensen disclosed a detection unit, arranged to detect in which of a plurality of ranges the instruction address lies, the detection unit being coupled to the instruction execution unit that parallelizes processing of the instructions from the instruction word, dependent on a detected range (Jensen: Figure 5 elements 522 and 524, column 14 lines 11-23)(Fisher: Column 5 lines 62-67 continued to column 6 lines 1-25)(The combination uses Jensen's method of mode switching to switch back and forth from executing high ILP instructions to executing low ILP instructions.).

The advantage of mode switching through detecting a range of addresses over Fisher's methods is that it allows for eliminating mode switching instructions and reducing time consuming interrupts to switch modes (Jensen: Column 3 lines 48-67

continued to column 4 lines 1-9)(Fisher: Column 6 lines 26-47). One of ordinary skill in the art would have been motivated by this advantage to implement the mode switching method of Jensen into the processor of Fisher. Thus, one of ordinary skill in the art would have been motivated by the advantages of reducing the program size and limiting the number of required interrupts to implement the method of mode switching of Jensen into the processor of Fisher.

10. As per claim 2:

Fisher and Jensen disclosed a data processing apparatus according to claim 1, wherein the instruction execution unit and/or the instruction memory system is arranged to adjust a width of the instruction word that determines a number of instruction from the instruction word that is processed in parallel (Fisher: Figure 2 elements 150A-D, column 5 lines 26-37 and column 6 lines 37-47)(The execution units execute full VLIW instructions or partial VLIW instruction dependent on the mode of the processor.), dependent on the detected range (Jensen: Figure 5 elements 522 and 524, column 14 lines 11-23)(Fisher: Column 5 lines 62-67 continued to column 6 lines 1-25)(The combination uses Jensen's method of mode switching to switch back and forth from executing high ILP instructions to executing low ILP instructions.).

11. As per claim 3:

Fisher and Jensen disclosed a data processing apparatus according to claim 1, wherein the instruction execution unit comprises a plurality of functional units (Fisher: Figure 2 elements 150A-D, column 5 lines 26-37), the instruction execution unit being arranged to select a subset of the functional unit that is available for processing the

instructions (Fisher: Figure 2 element 150D, column 6 lines 55-63)(The low ILP mode uses a subset of the function units available for processing.), dependent on the detected range (Jensen: Figure 5 elements 522 and 524, column 14 lines 11-23)(Fisher: Column 5 lines 62-67 continued to column 6 lines 1-25)(The combination uses Jensen's method of mode switching to switch back and forth from executing high ILP instructions to executing low ILP instructions.).

12. As per claim 4:

Fisher and Jensen disclosed a data processing apparatus according to claim 1, wherein the instruction execution unit comprises a plurality of functional units (Fisher: Figure 2 elements 150A-D, column 5 lines 26-37), the instruction execution unit being arranged to select whether functional units or groups of functional unit from a set of functional unit each receive respective instructions from the instruction word, or receive a shared instruction from the instruction word (Fisher: Figures 2-3, column 5 lines 62-67 continued to column 6 lines 1-25)(An individual functional unit is used in low ILP mode and the entire execution unit is used in high ILP mode.), dependent on the detected range (Jensen: Figure 5 elements 522 and 524, column 14 lines 11-23)(Fisher: Column 5 lines 62-67 continued to column 6 lines 1-25)(The combination uses Jensen's method of mode switching to switch back and forth from executing high ILP instructions to executing low ILP instructions.).

13. As per claim 5:

Fisher and Jensen disclosed a data processing apparatus according to claim 1, wherein the instruction memory comprises a first memory unit and a second memory

unit (Fisher: Figure 2 element 120 and 122, column 5 lines 54-61), providing storage with a first and second unit of width of addressable memory locations for instruction words of different lengths with addresses in a first and second range respectively, the first and second unit of width being mutually different (Fisher: Column 7 Line 15-26)(The low ILP and high ILP modes use different VLIW instruction lengths. The different instruction lengths are inherently located at different addressable memory location widths.).

14. As per claim 7:

Fisher and Jensen disclosed a data processing apparatus according to claim 5, comprising a memory mapping unit arranged to map the instruction address onto the first memory unit of the second memory unit, dependent on the detected range (Fisher: Column 5 lines 62-67 continued to column 6 lines 1-25)(The instructions are mapped to the main cache or the mini cache dependent on the range of the instruction being in a high ILP process or being in a low ILP process.).

15. As per claim 15:

Claim 15 essentially recites the same limitations of claim 1. Therefore, claim 15 is rejected for the same reasons as claim 1.

16. As per claim 16:

The additional limitation(s) of claim 16 basically recite the additional limitation(s) of claim 2. Therefore, claim 16 is rejected for the same reason(s) as claim 2.

17. As per claim 17:

The additional limitation(s) of claim 17 basically recite the additional limitation(s) of claim 3. Therefore, claim 17 is rejected for the same reason(s) as claim 3.

18. Claims 6 and 14 are rejected under 35 U.S.C. §103(a) as being unpatentable over Fisher et al. (U.S. 6,026, 479), in view of Jensen et al. (U.S. 7,149,878), further in view of Lilja et al. ("Exploiting the parallelism available in loops," IEEE, pages 13-26, February 1994).

19. As per claim 6:

Fisher and Jensen disclosed a data processing apparatus according to claim 5, programmed to execute a program, longer instruction words being stored in the first memory unit (Fisher: Figure 2 element 120, column 5 lines 62-67 continued to column 6 lines 1-7)(The high ILP instructions are longer in length than the low ILP instructions.), shorter instruction words being stored in the second memory unit (Fisher: Figure 2 element 120, column 6 lines 8-25)(The low ILP instructions are shorter in length than the high ILP instructions), the first unit of width being larger than the second unit of width (Fisher: Figure 2 elements 120 and 122, column 5 lines 62-67 continued to column 6 lines 1-25)(The high ILP instructions are wider instructions because they contain 4 operations compared to the single operation in low ILP instructions.).

Fisher and Jensen failed to teach longer instructions words coming from an inner loop and shorter instruction words from a majority of the program outside the inner loop.

However, Lilja disclosed longer instructions words coming from an inner loop and shorter instruction words from a majority of the program outside the inner loop (Lilja:

Page 13 lines 15-16)(Lilja disclosed that loops contain a larger amount of parallelism. Thus, it's obvious to one of ordinary skill in the art that the high ILP instructions are from loops and low ILP instructions are outside of loops.)

Lilja disclosed that most of the parallelism of a program is contained within loops (Lilja: Page 13 lines 15-16). One of ordinary skill in the art would have been motivated by this to put high ILP instructions from a loop into the main cache and low ILP instructions outside of a loop into the mini cache of Fisher. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement placing high ILP instructions coming from a loop and low ILP instructions coming from outside of loops into their respective caches because of the fact that most parallelism occurs within loops.

20. As per claim 14:

The additional limitation(s) of claim 14 basically recite the additional limitation(s) of claim 6. Therefore, claim 14 is rejected for the same reason(s) as claim 6.

21. Claims 8-9 are rejected under 35 U.S.C. §103(a) as being unpatentable over Fisher et al. (U.S. 6,026, 479), in view of Jensen et al. (U.S. 7,149,878), further in view of Maiyuran et al. (U.S. 2002/0129201).

22. As per claim 8:

Fisher and Jensen disclosed a data processing apparatus according to claim 5, wherein the instruction memory system is arranged to disable the first memory unit when addresses in the second range are detected (Fisher: Column 7 lines 15-37 and

column 8 lines 21-25)(Fisher disclosed deactivating the mini cache when instructions are being fetched from the main cache.).

Fisher and Jensen failed to teach disable supply of clock signals to the first memory.

However, Maiyuran disclosed disable supply of clock signals to the first memory (Maiyuran: Paragraph 28)(A cache is disabled by using clock signals.).

Fisher disclosed that caches can be deactivated when they are not being used to fetch instructions from, but didn't detail how the caches are actually deactivated. One of ordinary skill in the art would have been motivated by this lack of information to find Maiyuran that disclosed that caches can be disabled by using clock signals. Thus, it's obvious to one of ordinary skill in the art to implement the use of clock signals to disable the caches of Fisher when they aren't in use.

23. As per claim 9:

Fisher and Jensen disclosed a data processing apparatus according to claim 5, wherein the instruction memory system is arranged to disable all but the memory unit from whose address range addresses are detected (Fisher: Column 7 lines 15-37 and column 8 lines 21-25)(Fisher disclosed deactivating the mini cache when instructions are being fetched from the main cache.).

Fisher and Jensen failed to teach disable supply of clock signals to the first memory.

However, Maiyuran disclosed disable supply of clock signals to the first memory (Maiyuran: Paragraph 28)(A cache is disabled by using clock signals.).

Fisher disclosed that caches can be deactivated when they are not being used to fetch instructions from, but didn't detail how the caches are actually deactivated. One of ordinary skill in the art would have been motivated by this lack of information to find Maiyuran that disclosed that caches can be disabled by using clock signals. Thus, it's obvious to one of ordinary skill in the art to implement the use of clock signals to disable the caches of Fisher when they aren't in use.

24. Claims 10 and 12 are rejected under 35 U.S.C. §103(a) as being unpatentable over Fisher et al. (U.S. 6,026, 479), in view of Jensen et al. (U.S. 7,149,878), further in view of Sanches et al. (U.S. 2002/0116596).

25. As per claim 10:

Fisher and Jensen disclosed a data processing apparatus according to claim 2, wherein the instruction memory system comprises a plurality of memory units (Fisher: Figure 2 element 120 and 122, column 5 lines 54-61), each arranged to be responsive to instruction addresses in a respective range (Fisher: Figure 2 element 120 and 122, column 5 lines 54-61)(Jensen: Figure 4, column 13 lines 7-22)(Each memory stores a range of addresses.), the instruction memory system being arranged to supply the instruction word as a combination of instructions from those of the memory units in whose respective range the instruction address lies (Fisher: Figure 2 element 120, column 5 lines 27-37)(The high ILP instruction word is a combination of instructions that are stored in the main cache based on its instructions address.).

Fisher and Jensen failed to teach the instruction memory allowing partial overlap of the respective ranges.

However, Sanches disclosed the instruction memory allowing partial overlap of the respective ranges (Sanches: Paragraph 42)(Sanches allows for sequential in order program instructions to be stored in different memory banks.).

The advantage of the system of Sanches is that it allows for avoiding the storing of VLIW instructions that contain nop instructions (Sanches: Paragraph 15). The advantage of not using as many nop instructions in VLIW instructions is that the code size of the overall program is reduced. One of ordinary skill in the art would have been motivated by this advantage to implement the memory system of Sanches in Fisher. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the memory system of Sanches in Fisher for the advantage of reducing the storing of nop instructions.

26. As per claim 12:

Fisher, Jensen, and Sanches disclosed a data processing apparatus according to claim 10, wherein the execution unit comprises groups of one or more functional units (Fisher: Figure 2 elements 150A-D), each group being coupled to a respective predetermined one of the memory units, for receiving instructions from the instruction words (Fisher: Figure 2 elements 120 and 150A-D), when the instruction address is in the respective range of the respective predetermined one of the memory unit to which the group is coupled (Jensen: Figure 5 elements 522 and 524, column 14 lines 11-23)(Fisher: Column 5 lines 62-67 continued to column 6 lines 1-25)(The combination

uses Jensen's method of mode switching to switch back and forth from executing high ILP instructions to executing low ILP instructions.).

27. Claim 11 is rejected under 35 U.S.C. §103(a) as being unpatentable over Fisher et al. (U.S. 6,026, 479), in view of Jensen et al. (U.S. 7,149,878), further in view of Sanches et al. (U.S. 2002/0116596), further in view of Maiyuran et al. (U.S. 2002/0129201).

28. As per claim 11:

The additional limitation(s) of claim 11 basically recite the additional limitation(s) of claim 8. Therefore, claim 11 is rejected for the same reason(s) as claim 8.

Response to Arguments

29. The arguments presented by Applicant in the response, received on 7/9/2008 are not considered persuasive.

30. Applicant argues "Neither Fisher nor Jensen disclosed including at least one type of memory selected to achieve a desired instruction cycle time" for claims 1 and 15.

This argument is not found to be persuasive. Fisher disclosed using an instruction cache to store the instructions. The use of a memory cache is for achieving faster memory access times so that instructions can be accessed faster than if they were fetched from main memory. Thus, the use of instruction caches reads upon the claimed limitation.

The examiner notes that on page 6 lines 6-9 of the specification, support for an amendment is given that would likely overcome the rejection of Fisher and Jensen. The specification here disclosed that the first of the memory units may be faster than the second memory units. Fisher disclosed in column 8 lines 41-65 the use of direct-mapped caches and set-associative caches, where both the main and mini caches are using the same type of memory. One of ordinary skill in the art would realize that the memory speed for each type of cache would be the same for the main and mini cache regardless of the size of each. Thus, such an amendment for the two memories storing the short and long instruction would likely overcome the combination.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183

Jacob Petranek
Examiner, Art Unit 2183